

**Remarks/Arguments**

Reconsideration of this application is requested.

**Claim Status**

Claims 1-23 were presented. Claims 1-11 are canceled, without prejudice, as a result of the election of claims 12-23 which remain pending. Claims 12 and 16-23 are amended.

**Specification**

The Action objects to the specification because of a misspelling of "device" at page 14, line 18. In response, the misspelling is corrected.

**Claim Objections**

The Action objects to claims 17-22 and suggests that "a semiconductor" be changed to "the semiconductor". The suggested change is made. The Action also objects to claim 23 because of a clerical error. The error is corrected as suggested.

**Claim Rejections – 35 USC 112**

Claims 12-15 are rejected under 35 USC 112 as indefinite as they depend from non-elected and now canceled claim 1. In response, claim 12 is amended to be an independent apparatus claim. Claims 13-15 depend from claim 12.

**Claim Rejections – 35 USC 102**

Claims 12-15 are rejected under 35 USC 102(b) as anticipated by Tachibana (USP 5,889,323). Claims 12-23 are rejected under 35 USC 102(b) as anticipated by Salatino (USP 5,798,557). In response, independent claims 12, 16 and 23 are amended to clearly distinguish over Tachibana and Salatino.

The present application is directed to a cover (10) for a semiconductor substrate. A first opening (12) is formed in the cover to hold an adhesive (40), and a second opening (14) is formed in the cover to enclose an electrode or optical unit on the semiconductor substrate. Importantly, the adhesive is contained entirely within and does not leak outside of the first opening (see, e.g., paragraph 53 of applicant's specification). This permits the sealing of the electrode or optical unit within the second opening (14) without exposure to the adhesive (40).

Tachibana discloses a cap 14 for covering a semiconductor chip 11. Cap 14 includes a depression area 14a above chip 11. Chip 11 is affixed to depression area 14a by resin 15. Resin 16 is used to seal the outer circumference of cap 14 to case 13. Importantly, and as clearly seen in Tachibana's drawing figures, resin is present in the opening that contains chip 11 and indeed contacts chip 11. Moreover, the resin 16 applied to the outer portions of cap 14 is not sealed from the opening containing chip 11 and is therefore free to leak into the opening containing chip 11.

Salatino discloses first and second openings 263, 264, 265 formed in an insulating layer 262 of cover 260. The Action asserts that insulating layer 262 is an adhesive similar to adhesive 40 of the present invention. Applicant disagrees. According to Salatino, insulating layers 262 and 236 are brought into contact and heated to bond cover (lid wafer) 260 to wafer 200. *See Salatino, Col. 3, lines 39-41.* There is no adhesive contained entirely within a first opening that seals an element contained within a second opening.

Independent claims 12, 16 and 23 are amended to include this distinguishing subject matter. Claim 12 requires a "first opening configured so that adhesive is present only in the first opening and not in the second opening". Claim 16 requires that the "second opening that includes the optical unit is sealed from the adhesive in the first opening". Claim 23 requires that the adhesive is "sealed within the first opening and not present in the second opening".

Since neither Tachibana nor Salatino discloses or suggests these claim limitations, they cannot anticipate claims 12, 16, 23, or those claims dependent thereon. For these reasons, the rejections of claims 12-23 based on Tachibana and Salatino should be withdrawn.

### **Conclusion**

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This application is now in condition for allowance. The Examiner is invited to telephone the undersigned to resolve any issues that remain after entry of this amendment. Any fees due in connection with this response may be charged to our Deposit Account No. 50-1314.

Respectfully submitted,  
HOGAN & HARTSON L.L.P.

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By: \_\_\_\_\_

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